IN THE DRAWINGS

Please approve the changes to Fig. 2 as indicated in red on the sheet attached to the accompanying Letter to the Official Draftsman.

IN THE CLAIMS

Please cancel claim 5 without prejudice as to the subject matter underlying this claim.

Please amend claims 3, 6, 13, and 21 as follows:

3. (Twice Amended) A voltage doubler receiving at an input a continuous power voltage and supplying at an output a voltage having a value virtually double that of said continuous power voltage, the voltage doubler comprising:

a. an oscillator powered by said continuous power voltage and having two outputs in phase opposition,

b. a charge accumulation condenser having a first terminal connected to a potential reference and a second terminal connected to the output of the doubler,

c. a first charge transfer condenser and a second charge transfer condenser having first terminals respectively connected to the outputs of said oscillator,

d. a bridge comprising four transistors and corresponding bulk diodes of the transistors, the transistors being arranged so that the four bulk diodes for a

bridge, having a positive terminal connected to the second terminal of said charge accumulation condenser, a negative terminal connected to said continuous power voltage and two intermediate terminals respectively connected to second terminals of said first charge transfer condenser and said second charge transfer condenser, and

B1 Cnt. [e.] the four transistors having principal conduction paths connected in parallel with said four diodes and control terminals connected to the first charge transfer condenser and the second charge transfer condenser in such a way as to lower a voltage drop along branches of the bridge when the doubler reaches a steady state.

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6. (Twice Amended) A voltage booster receiving at an input a continuous power voltage and supplying at an output a voltage higher than the continuous power voltage, the voltage booster comprising:

a. an oscillator powered by said continuous power voltage, having two outputs in phase opposition,

B2 b. a charge accumulation condenser having a first terminal connected to a first potential reference and a second terminal connected to the output of the booster, and

c. at least one charging section having a charge output terminal, a power input

terminal, a first side terminal and a second side terminal respectively connected to the outputs of said oscillator, and said at least one charging section being connected in series with the output terminal connected to the second terminal of said charge accumulation condenser and the input terminal connected to [a] the continuous power voltage,

wherein the at least one charging section comprises:

a first charge transfer condenser and a second charge transfer condenser having respective first terminals connected to said first and second side terminals, and

a bridge of controlled switches having two [indifferent] intermediate terminals connected to respective second terminals of said first charge transfer condenser and said second charge transfer condenser, a negative terminal connected to said power input terminal and a positive terminal connected to said charge output terminal ,

and wherein the value of the voltage of the output corresponds to <u>said continuous power voltage</u> [said second potential less the value of said first potential] plus the product of said continuous power voltage and a number of the at least one charging section.

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13. (Twice Amended) An electrically programmable and delectable non-volatile memory device of a type powered with a low voltage comprising:

a. an oscillator powered by said low voltage, having two outputs in phase opposition,

b. a charge accumulation condenser having a first terminal connected to a first potential reference and a second terminal connected to an output of the memory device, and

c. at least one charging section having a charge output terminal, a power input terminal, a first side terminal and a second side terminal respectively connected to the outputs of said oscillator and said at least one charging section being connected in series with the output terminal connected to the second terminal of said charge accumulation condenser and the input terminal connected to the low voltage,

wherein the at least one charging section comprises:

B3 Cont.

a first charge transfer condenser and a second charge transfer condenser having respective first terminals connected to said first and second side terminals, and

a bridge of controlled switches having two intermediate terminals connected to respective second terminals of said first charge transfer condenser and said second charge transfer condenser, a negative terminal connected to said power input terminal and a positive terminal connected to said charge output terminal,

and wherein the value of the voltage of the output corresponds to <u>said continuous power voltage</u> [said second potential less the value of said first potential] plus the product of said continuous power voltage and a number of the at least one charging section.

14. (Twice Amended) A voltage regulator having a low voltage drop between an input and an output of a type having a MOS power transistor as an output regulation element and a voltage booster means having an output coupled to a control terminal of said power transistor to maintain a conduction condition on the power transistor when operating conditions of the regulator change, wherein the voltage booster means includes:

a. an oscillator powered by a continuous power voltage, having two outputs in phase opposition,

b. a charge accumulation condenser having a first terminal connected to a first potential reference and a second terminal connected to the output of the voltage booster means, and

B3 Cont.

c. at least one charging section having a charge output terminal, a power input terminal, a first side terminal and a second side terminal respectively connected to the outputs of said oscillator and said at least one charging section being connected in series with the output terminal connected to the second terminal of said charge accumulation condenser and the input terminal connected to [a] the continuous power voltage,

wherein the at least one charging section comprises:

a first charge transfer condenser and a second charge transfer condenser having respective first terminals connected to said first and second side terminals, and

a bridge of controlled switches having two intermediate terminals connected to respective

second terminals of said first charge transfer condenser and said second charge transfer condenser, a negative terminal connected to said power input terminal and a positive terminal connected to said charge output terminal ,

B3 Cont.

and wherein the value of the voltage of the output corresponds to said continuous power voltage [said second potential less the value of said first potential] plus the product of said continuous power voltage and a number of the at least one charging section.

18 ~~21~~. (Twice Amended) The voltage multiplier of claim 16 ~~19~~, wherein the at least one bridge circuit includes:

four diodes in a bridge arrangement such that a positive terminal is connected to the output of the bridge circuit, a negative terminal is connected to the input of the bridge circuit, and two intermediate terminals are connected to the side inputs of the bridge circuit; and

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four transistors having principal conduction paths connected in parallel with the four diodes and control terminals connected to the side inputs.

19 ~~22~~. (Twice Amended) The voltage multiplier of claim 17 ~~20~~, wherein each of the plurality of series connected bridge circuits includes:

four diodes in a bridge arrangement such that a positive terminal is connected to the output of the bridge circuit, a negative terminal is connected to the input of the bridge circuit, and two intermediate terminals are connected to the side inputs of the bridge circuit; and

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B4 Cont. four transistors having principal conduction paths connected in parallel with the four diodes and control terminals connected to the side inputs.

REMARKS

In response to the Office Action mailed August 12, 1996, Applicants respectfully request reconsideration. The drawings were objected to because of informalities. Claims 1-25 were rejected under 35 U.S.C. § 112, first paragraph, as not being enabled. Claims 3-14, 21-22 and 25 were rejected under 35 U.S.C. § 112, second paragraph as being indefinite. Claims 1-11, 13-14, 16-19, 21 and 24 were rejected under 35 U.S.C. § 102(b) as being anticipated by Matsumura, under 35 U.S.C. § 102(b) or § 103 as being anticipated by or obvious over Okada. Claims 20, 22, and 25 were rejected under 35 U.S.C. § 103 as being obvious over Matsumura or Okada. In light of the above amendments, Applicants respectfully traverse these rejections.

Changes to the drawings have been presented for approval to correct the informalities suggested in the Office Action. Therefore, the objection to the drawings has been overcome.

With respect to the rejection under 35 U.S.C. § 112, first paragraph, applicants respectfully suggest that the Office Action is incorrect in the interpretation of the drawings and the specification. First, the Office Action suggests that the diodes in the figures show the body and drain short-circuited together, instead of the body and source. Applicants respectfully suggest that the arrangement of the transistors has been misunderstood. Bulk diodes in a MOSFET are drawn between the source and gate, which represent the body effect. Applicants